Name:

Enrolment No:

UPES

End Semester Examination, December 2024

Programme Name: B. Tech (Electronics & Communication Engineering) / Electronics & Computer Engineering)

Course Name : VLSI Design **Time : 03 Hrs**

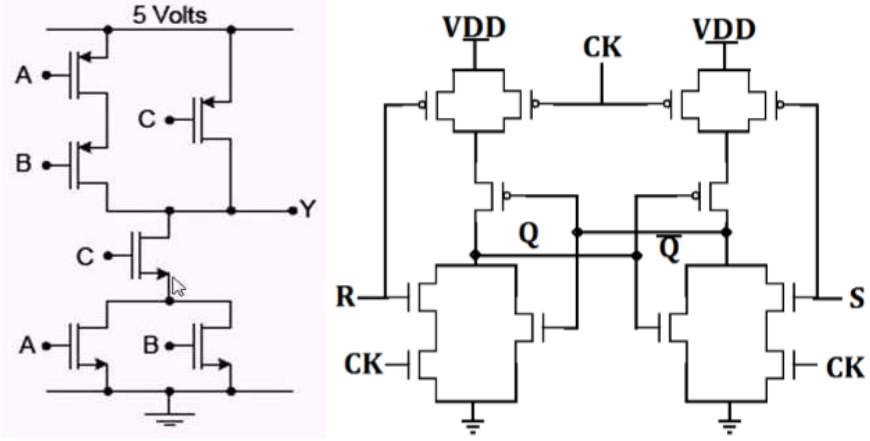
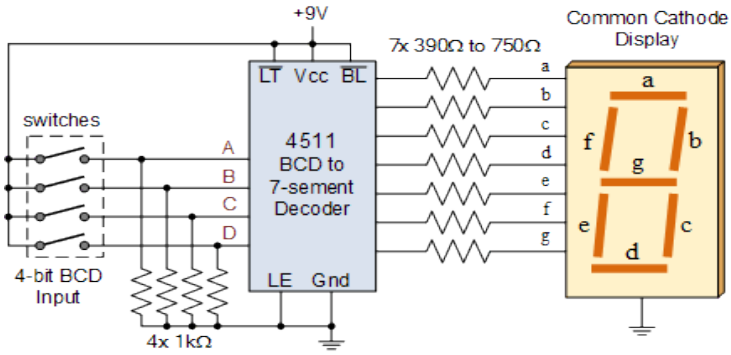
Course Code : ECEG-3049 **Max. Marks : 100**

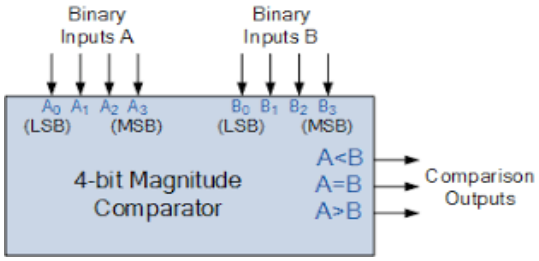
Nos. of page(s) : 02 **Semester : V**

Instructions: Assume any data in programming, if required.

SECTION A (4 x 5 = 20 Marks)

Attempt *all* the questions

S. No.		Marks	CO
Q.1	Discuss the ASIC Design Flow in detail and detail the different abstraction levels in ICs with example.	**5**	**CO1**
Q.2	Realize the output of the logic diagram shown in Fig. 1  (a) (b) Fig. 1 CMOS Realization	**5**	**CO3**
Q.3	What are the different styles of modeling followed in VHDL based design. Design a full adder using data flow and behavioral model.	**5**	**CO4**
Q.4	Draw the logic diagram and functional table to support common cathode display of the 7-segment display (0 to 9) and develop the code in VHDL programing language to support the same functionality.  Fig.2 Common Cathode -7 Segment Display	**5**	**CO5**

SECTION B (4 x 10 = 40 Marks) **Attempt *all* the questions**			
Q.5	(a) Explain the concept of propagation delay and Noise Margin with examples in MOSFET circuits. (b) Realize the following functions using NMOS and CMOS. $Y = \overline{A.(B + CD)}$ $Y = \overline{X + Y + Z}$	**10**	**CO2**
Q.6	What is the significance of stick diagram and layout diagram for understanding MOSFET design? Draw the stick diagram and layout design of 2 input NAND and XOR gate based on CMOS logic. ***OR*** Detail the fabrication process of **npn-BJT** transistor.	**10**	**CO3**
Q.7	Detail the functionality of enhancement type NMOS/PMOS under different regions. Explain the drain voltage characteristics and transfer characteristics in detail	**10**	**CO1**
Q.8	Draw the voltage transfer curve for the NMOS/CMOS inverter and derive the mathematical expression to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for NMOS/CMOS inverter circuit and detail the functionality.	**10**	**CO2**
SECTION-C (2 x 20 = 40 Marks) **Attempt *any two* the followings**			
Q.9	**(a)** Draw the cross-sectional view of CMOS. Detail all the steps and fabrication process of CMOS using P-Well Process. **(b)** Draw the FPGA design flow used for synthesis the logic. Draw the architecture of any one of the FPGA and explain the functionality: XC 3000, SPARTAN 6, Virtex 7.	**10+10**	**CO3**
Q.10	**(a)** Consider a process technology for which L_{min} = 0.4 μm, tox = 8 nm, μ_n = 450 cm^2/ V-s and V_t = 0.7 V **(i)** Find C_{ox} and K'_n **(ii)** For a MOSFET with W/ L = 8 μm/0.8 μm, Calculate the value of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_D =100μA. **(iii)** For the same device, find the value of V_{GS} required to cause the device to operate as a 1000 Ω resistor for very small V_{DS}. (b) Derive the mathematical equation of PMOS/NMOS for saturation and active regions.	**10+10** **10+10**	**CO4**
Q.11	**(a)** Design the chip using VHDL/ Verilog HDL that supports the following behaviour.  **(b)** Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA.	**10+10**	**CO5**