| Name:

Enrolment No: |
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UPES
End Semester Examination, May 2024
Course: Computer System Architecture
Semester: IV
Program:BCA-CSF/AIML   **Time   : 03 hrs.**
Course Code: CSEG 2004P   **Max. Marks: 100**

Instructions:

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Describe Von Neuman architecture with schematic diagram.	4	CO1
Q 2	Write down the truth table and characteristics table of a JK flip-flop.	4	CO1
Q 3	Write in brief, the process of fetching, decoding and executing of an instruction.	4	CO2
Q 4	Write a short note on cache memory.	4	CO1
Q 5	Write a short note on superscalar processor.	4	CO3

SECTION B
(4Qx10M= 40 Marks)

Q 6	Differentiate between micro programmed vs. hardwired control unit.	10	CO3
Q 7	What are direct and indirect mode of memory access? Discuss in detail.	2+8	CO2
Q 8	With the help of necessary diagram, design the control unit of a basic computer that has 4Kof main memory and 16 bit shared bus. Give necessary explanations, where necessary.	10	CO3
Q 9	Describe in detail how static memory is different from dynamic memory.
OR
Discuss in details, the working of auxiliary memory.	10	CO4

SECTION-C
(2Qx20M=40 Marks)

| Q 10 | Describe the process of bus arbitration with detailed diagram.
Describe the process of Direct Memory Access with necessary diagrams. | 10+10 | CO5 |
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| Q 11 | Give a detailed study of different types of interrupts with necessary diagrams | 20 | CO5 |