**Name:**

**Enrolment No:**

UPES
UNIVERSITY WITH A PURPOSE

**UNIVERSITY OF PETROLEUM AND ENERGY STUDIES**
**End Semester Examination, June 2021**

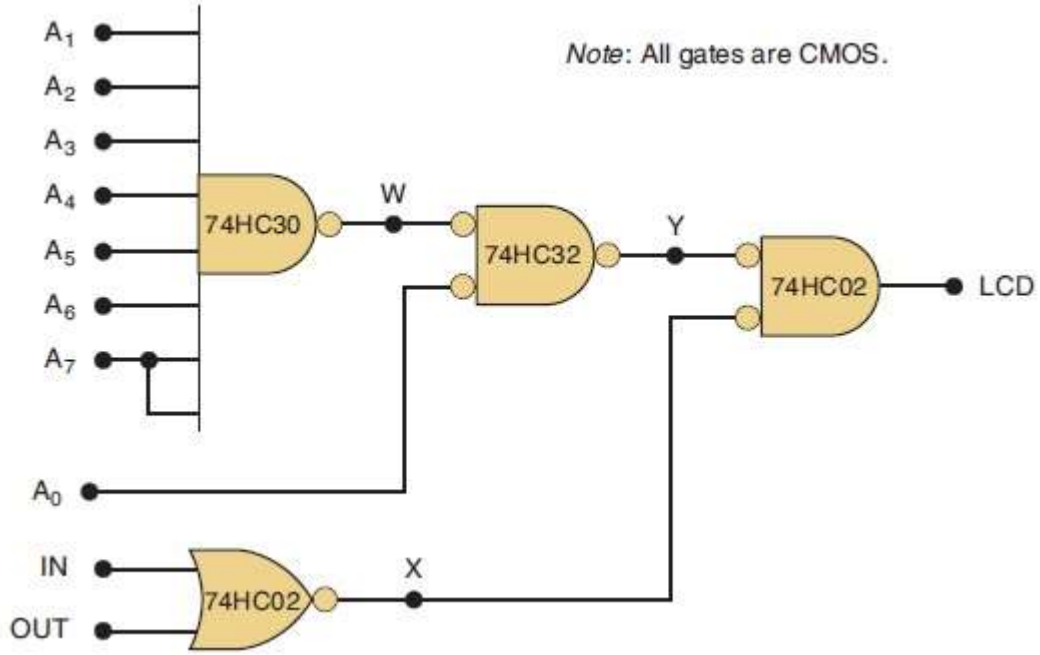
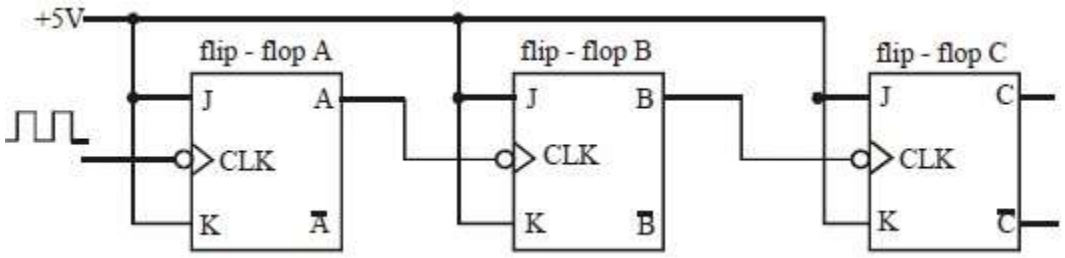
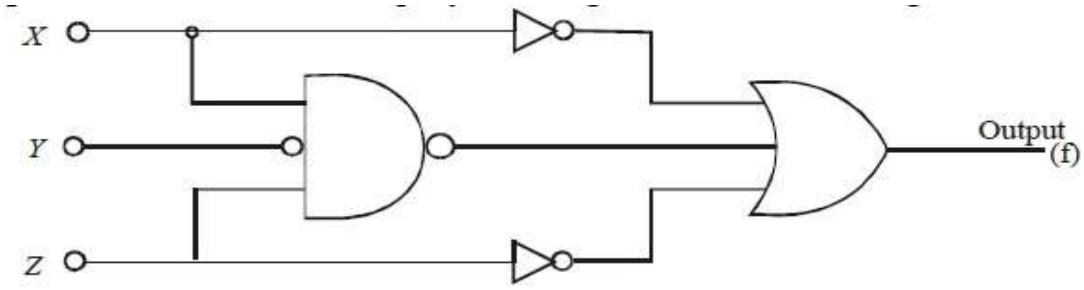
**Course:** Computer System Architecture — **Semester: II**
**Program:** B.Tech-CSE — **Time : 03 hrs.**
**Course Code:** CSEG1014 — **Max. Marks: 100**

**Instruction: Attempt all questions. Internal choice is given, where ever applicable.**

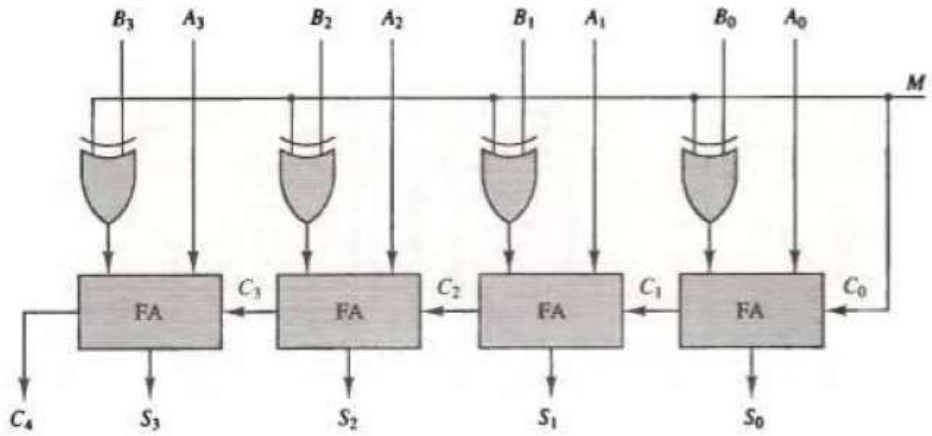
**SECTION A**

**1.** Each Question will carry 5 Marks

| S. No. | | Marks | CO |
|---|---|---|---|
| Q 1 | Reduce the following using Boolean Algebra (Type **A'** in place of $\overline{A}$ wherever applicable.)<br>$(i)\ Z = A\,[B + C(AB + AC)]$<br>$(ii)\ Z = \overline{A}\,\overline{B}\,C + \overline{(A + B + C)} + \overline{A}\,\overline{B}\,\overline{C}D.$ | **2.5 + 2.5 = 5** | **CO2** |
| Q 2 | Convert the following as indicated by their base: (Type only the final answer).<br>$(i)\ \ (650)_{10} \rightarrow (\ \ )_{16}$<br>$(ii)\ \ (CA57)_{16} \rightarrow (\ \ )_{2}$<br>$(iii)\ (7BF)_{16} \rightarrow (\ \ )_{2}$<br>$(iv)\ \ (110101)_{2} \rightarrow (\ \ )_{8}$<br>$(v)\ \ (E7F6)_{16} \rightarrow (\ \ )_{10}$ | **1 X 5 = 5** | **CO2** |
| Q 3 | Name the *addressing modes* involved in the following operations:<br>(i) Pointer<br>(ii) Program Relocation<br>(iii) Array Operation<br>(iv) Stack Operation<br>(v) Constant assignment. | **1 X 5 = 5** | **CO3** |
| Q 4 | Differentiate<br>(i) Hardwired control unit vs. Microprogrammed control unit.<br>(ii) CISC vs. RISC | **2.5 + 2.5 = 5** | **CO3** |
| Q 5 | The logic circuit shown below enables the liquid crystal display (LCD) of a handheld electronic device when the microcontroller is sending data to or receiving data from the LCD controller. The circuit will enable the display when LCD = 1. Determine the input conditions necessary to enable the LCD. | **5** | **CO1** |

| | | | |
|---|---|---|---|
| |  | | |
| Q 6 | What would be the MOD number of the counter be if three more flip-flops were added to the 3-bit asynchronous (or ripple) counter circuit shown below<br>  | **5** | **CO2** |
| **SECTION B**<br>**1. Each question will carry 10 marks** | | | |
| Q 7 | Determine the output (f) for the logic circuit shown below. Minimize the output (f) function using Boolean algebra and sketch the minimized logic circuit<br>  | **4+4+2 = 10** | **CO2** |
| Q 8 | Reduce the following function using **K map** and realize using *NAND gates* only.<br>$f(ABC) = AB\overline{C} + \overline{A}\overline{B}C + ABC + A\overline{B}C$ | **5+5 =10** | **CO2** |

<table>
<tr><td>Q 9</td><td>(i) Explain about priority based interrupt system.<br>(ii) Differentiate between vectored and non-vectored interrupt.<br>(iii) What is the main disadvantage of polling?<br>(iv) Briefly explain about DMA?</td><td>3+2+2 +3 =10</td><td>CO4</td></tr>
<tr><td>Q 10</td><td>(i) What is content addressable memory?<br>(ii) A digital computer has a memory unit of (64K X 16) and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.<br>(a) How many bits are there in the tag, index, block, and word fields of the address format?<br>(b) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.<br>(c) How many blocks can the cache accommodate?</td><td>2+3+3 +2 =10</td><td>CO4</td></tr>
<tr><td>Q 11</td><td>Explain the following<br>(i) Instruction Cycle<br>(ii) Fetch Cycle<br>(iii) Execution Cycle<br>(iv) Instruction Format<br>(v) Types of Instructions</td><td>2 X 5 = 10</td><td>CO1</td></tr>
<tr><td colspan="4">SECTION-C<br>Each Question carries 20 Marks.</td></tr>
<tr><td>Q 12</td><td>(i) Explain in detail about the various addressing modes.<br>(ii) Write a sequence of assembly level instructions that will compute the value of {x =(A +B) * (C + D)} using<br>(a) Three-address instructions<br>(b) Two-address instructions<br>(c) One-address instructions</td><td>10+ 10 = 20</td><td>CO3</td></tr>
<tr><td colspan="4">OR</td></tr>
<tr><td></td><td>(iii)Write short notes on<br>(a) Memory Address Register (MAR)<br>(b) Memory Data Register (MDR)<br>(iv)The adder-subtractor circuit shown below has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs: S3, S2, S1, S0, and C4<br><br><table><tr><td></td><td>M</td><td>A</td><td>B</td></tr><tr><td>a</td><td>0</td><td>0111</td><td>0110</td></tr><tr><td>b</td><td>0</td><td>1000</td><td>1001</td></tr><tr><td>c</td><td>1</td><td>1100</td><td>1000</td></tr><tr><td>d</td><td>1</td><td>0101</td><td>1010</td></tr><tr><td>e</td><td>1</td><td>0000</td><td>0001</td></tr></table><br>PTO</td><td>5 +5 + 10 =20</td><td>CO3</td></tr>
</table>


$B_3$
$A_3$
$B_2$
$A_2$
$B_1$
$A_1$
$B_0$
$A_0$
M
FA
FA
FA
FA
$C_3$
$C_2$
$C_1$
$C_0$
$C_4$
$S_3$
$S_2$
$S_1$
$S_0$