Name:

Enrolment No:



UNIVERSITY OF PETROLEUM AND ENERGY STUDIES End Semester Examination, April/May 2018

SET-1

Course: Analog Electronics-I (ECEG 2011)

Program: B.Tech ECE

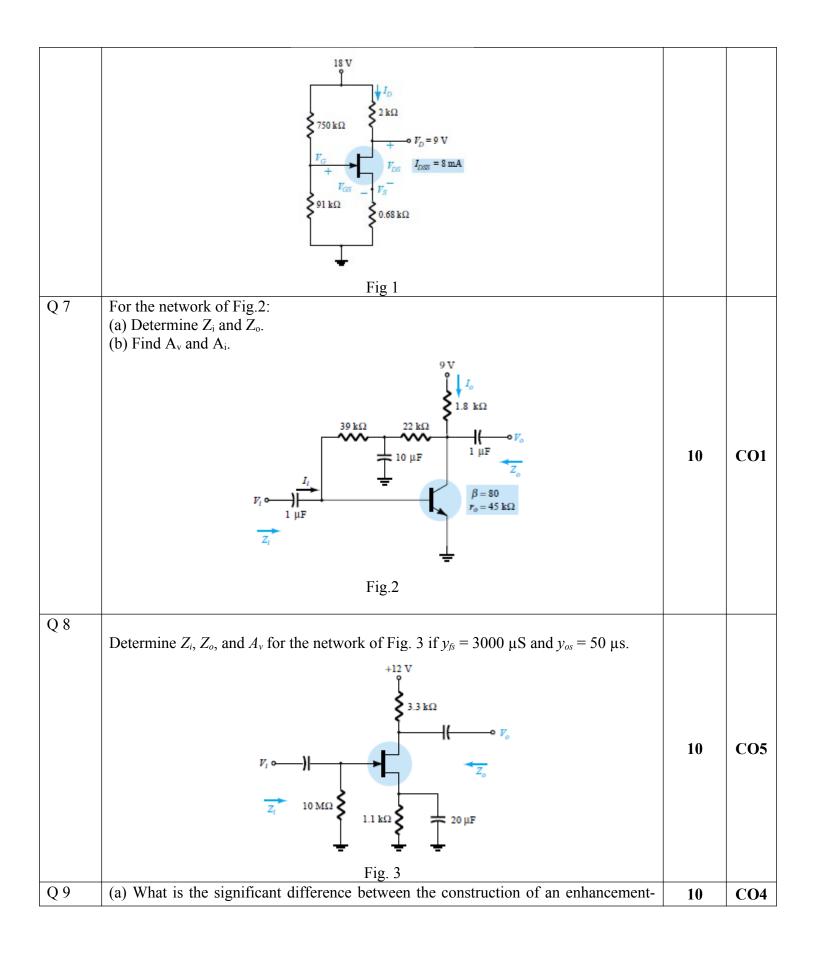
Time: 03 hrs.

Semester: IV

Max. Marks: 100

SECTION A

S. No.		Marks	CO
Q 1	Define I_{CBO} and I_{CEO} . How are they different? How are they related? Are they typically close in magnitude?	4	CO1
Q 2	What will happen to the output AC signal if the DC level is insufficient? Sketch the effect on the waveform.	4	CO1
Q 3	Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.	4	CO3
Q 4	What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable.	4	CO3
Q 5	What is the reactance of a 10-µF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilo-ohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?	4	CO2
	SECTION B		
Q 6	For the network of Fig. 1, $VD = 9 V$. Determine: (a) I_D . (b) V_S and V_{DS} . (c) V_G and V_{GS} . (d) V_P .	10	CO2

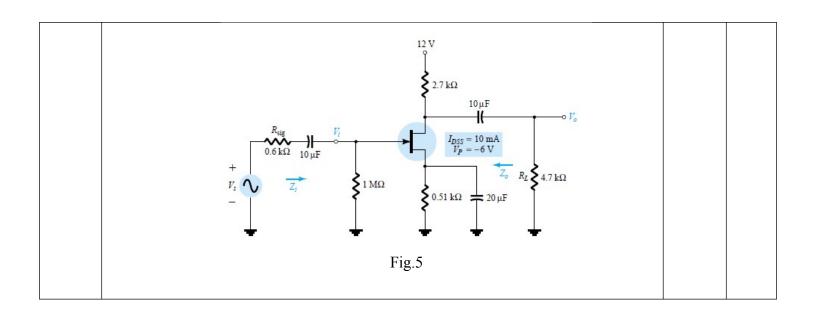


type MOSFET and a depletion-type MOSFET? (b) Sketch a p-channel enhancement-type MOSFET with the proper biasing applied $(V_{DS} > 0 \ V, \ V_{GS} = V_T)$ and indicate the channel, the direction of electron flow, and the resulting depletion region.					
SECTION-C					

Q 11 Given the typical values of $h_{ie} = 1 \text{ k}\Omega$, $h_{re} = 2 \times$

 10^{-4} , and $A_v = -160$ for the input configuration of Fig. 4:

(a) Determine V_o in terms of V_i . (b) Calculate I_b in terms of V_i . (c) Calculate I_b if $h_{re}V_o$ is ignored. (d) Determine the percent difference in I_b using the following equation: $\frac{I_b (withouth_{re}) - I_b (withh_{re})}{I_b (withouth_{re})} \times 100\%$ (e) Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example? hie Tight No. 100% Vi Pig.4	CO)3
Q 12 For the self-bias JFET network of Fig.5:	20	CO5
(a) Determine A_{vNL} , Z_i , and Z_o .		
(b) Sketch the two-port model with the parameters determined in part (a) in place.		
(c) Determine A_v and A_{vs} .		
(d) Change R_L to 6.8 k Ω and R_{sig} to 1 k Ω and calculate the new levels of Av and Avs .		
How are the voltage gains affected by changes in R_{sig} and R_L ?		
(e) For the same changes as part (d), determine Z_i and Z_o . What was the impact on		
both impedances?		



Name:

Enrolment No:



Semester: IV

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES End Semester Examination, April/May 2018

SET-2

Course: Analog Electronics -I (ECEG 2011)

Program: B.Tech ECE

Time: 03 hrs.

Max. Marks: 100

SECTION A

S. No.		Marks	CO
Q 1	Can you think of the analogy that would explain the importance of the DC level on the resulting AC gain?	4	CO1
Q 2	In general, comment on the polarity of the various voltages and direction of the currents for an n-channel JFET versus a p-channel JFET.	4	CO2
Q 3	With the help of small signal transistor model define the phase relationship of input and output waveform. Define the above statement with the valid equations.	4	CO1
Q 4	Describe in your own words why I _G is effectively zero amperes for a JFET transistor.	4	CO5
Q 5	Why is the terminology field effect appropriate for this important three-terminal device FET?	4	CO4
	SECTION B		
Q 6	Determine Z_i , Z_o , and V_o for the network of Fig. 1 if V_i = 20 mV. $V_i \circ \frac{1}{Z_i} = \frac{12 \text{ mA}}{V_p = -3 \text{ V}} V_{r_d} = \frac{100 \text{ k}\Omega}{Z_o}$	10	CO2
Q 7	Fig 1 For the common-base network of Fig. 2: (a) Determine Zi and Zo. (b) Calculate Av and Ai.	10	CO4

(c) Determine α , β , r_e , and r_o .

