EXECUTIVE SUMMARY

This dissertation considers two OFDMA systems. One being the conventional OFDMA and the other being the FFT window positioned OFDMA. In the conventional OFDMA the mitigation of the Inter Symbol Interference (ISI) which is caused by the multi path propagation of the symbols is done by Equalization techniques. On the other hand, the FFT window positioned OFDMA positions the FFT window at the receiver w.r.t the delay of symbols and the FFT operation is started only after all the symbols have been arrived at the receiver. The overview of the mitigation techniques of the ISI have been studied in the literature review. The OFDMA technology works by splitting the signal into multiple smaller sub-signals or sub-channels which are orthogonal to each other and that are transmitted simultaneously at different frequencies to the receiver. In time domain, the sub-channels are in rectangular pulses next to each other. On the other hand, these sub-channels are in sinc pulses in frequency domain. The peak amplitude of the sinc pulse is at nulls of other sinc pulse. By having this property, the orthogonality is achieved. To combat the interference of the symbols caused by the multi path fading and time dispersive channel, guard interval (GI) which is the length of cyclic prefix (CP) is implemented in an OFDMA system. To overcome interference between each symbols, the guard time must be set at least four times larger than the expected delay spread. It should be considered that the chosen duration of the guard time must be optimum; otherwise, the OFDM transmission will lose substantial power. The other aspects of orthogonality between the symbols and the cyclic prefix are discussed in the chapter 2.

In the physical layer of the OFDMA, FFT is the one of the important operations to perform. 2D-FFT algorithm has been implemented over FFT to improve the system level parallelism and the efficient use of the band width. To implement the same on the FPGA hardware, fixed point encoding and the floating point encoding of numbers is studied. Adder, Multiplier, Twiddle factor and the Butterfly structure are the main building of any FFT or IFFT operation. The

butterfly structure again depends upon type of decimation i.e. Decimation in Time (DIT-FFT) or Decimation in Frequency (DIF-FFT). The number of inputs of FFT N are divided into two shorter length FFT's i.e. $N=N_1xN_2$ to compute the FFT faster. In which N_1 = 64-pt FFT is fixed and the N_2 can be 2-pt FFT, 8-pt FFT, 16-pt FFT or 32-pt FFT. Ping-pong memory architecture can be used to store the real and imaginary values of the FFT input and outputs. Instead of manually giving the 2048 input points to the FFT processor, Direct Digital Synthesizer can be used to generate a sine signal in which all the input points are covered during the implementation of the FFT. The results can be viewed on the chipscope of the Xilinx ISE tool. The implementation aspects of the variable length 2D-FFT processor for OFDMA system is discussed in the chapter 3.

Although there are many modulation techniques used by OFDM systems, a common and simple technique is to use binary pulse shift keying (BPSK) signaling. Incoming signal is modulated to +1 and -1 before transmission and recovered back to the original signal after demodulation in the receiver. But this type of modulation limits bandwidth usage. The other technique is to use M-ary QAM. A 2 bit per OFDM symbol can be performed using 4-QAM. The data signal is mapped into 4 levels which are $\pm 1 \pm j$. At the receiver, the signal needs to be detected and demodulated for recovery. Performance analysis with respect to BER of digital modulation schemes with different order can be done to choose the best digital modulation scheme. The more the levels of QAM, the more complex the receiver needs to demodulate for the recovery. This will result more bit errors as the system becomes more complex. Another important aspect is channel selection for the implementation of the system. The channels were simulated and BER was calculated for the AWGN, Rayleigh and Rician fading channels. There is also need to observe the characteristics of the channel with the increase in the input FFT points. The multiple symbols get combined at the receiver antenna of the mobile to produce a composite received signal. The wavelength of the carrier used in Ultra High Frequency (UHF) mobile radio applications typically ranges from 15 to 60 cm. Therefore, even the small change

in the differential propagation delay will cause large changes in the phases of the individually arriving plane waves at the receiver. Delay spread, Doppler spread, Coherence Time and Coherence Bandwidth are the main parameters on which the characteristics of multi-path channels depend. These multipath channel parameters are derived from the power delay profile of the received signal. The time dispersive properties of wide band multipath channels are most commonly calculated by their mean excess delay ($\overline{\tau}$) and RMS delay spread (σ_{τ}). Chapter 4 gives the detailed analysis of the digital modulation scheme, channel selection and the delay spread.

Apart from the better receiver and transmitter technology, the OFDM/A communication requires better signal processing techniques to improve the link performance. One such signal processing technique is equalization which is used to compensate the Inter Symbol Interference (ISI) created by multipath transmission within time dispersive channels. Equalizer is actually the inverse filter of the channel. Zero forcing equalizer is the simplest equalizer but a generic adaptive equalizer is used in general. Since the main task of an adaptive equalizer is to compensate for unknown and time varying channel, a tracking loop system i.e. specific algorithm is needed to update the coefficients and track the channel variations. Least Mean Square (LMS) algorithm, Recursive Least Square (RLS) algorithm and Constant Modulus Algorithm (CMA) are simulated and the BER analysis and comparisons are shown in the chapter 5.

The proposed technique and its hardware implementation and its comparison with the conventional OFDMA are discussed in chapter 6. The brief device utilization, HDL synthesis report of the vertex-5 FPGA board along with the timing summary is presented here. The delay provided by the ITU delay profiles for ideal delay case, pedestrian delay case and vehicular delay cases have been considered for the simulation and synthesis of the FFT window positioning of the OFDMA. The top view representation of a design is the Register Transfer Level (RTL) view which depicts the pin details and input and output of the system. Integrated Controller Core

(ICON core) is the core which uses the JTAG Boundary Scan port to communicate to the host computer via a JTAG download cable. Integrated Logic Analyzer (ILA core) is a customizable logic analyzer core that can be used to monitor any internal signal of the design.16-bit input length registers have been used in which 10-bits are considered for the fractional part. The simulation as well as the synthesis results with input and the output wave forms of the FFT window positioned OFDMA can be observed in chapter 7. The BER comparisons of conventional OFDMA and the proposed window positioned OFDMA have been carried out in the same.

I hope that this dissertation would be used as a source of study and inspire further research in these fields.