Chapter 7

Conclusions and Future Directions

The purpose of this chapter is to bring out the summary of each chapter and the overall thesis results and also to include considerable future scope directions. The second and third chapters discussed about Fourier based OFDMA and the implementation of variable length FFT processor on FPGA kit. The results are included with the orthogonality in the subcarriers, cyclic prefix, and 2DFFT algorithm. As the size of the FFT points increases (in the case of OFDMA 2048-pt FFT implementation) efficient way of implementing the same on hardware is to make use of 2D-FFT algorithm in which the input point N is again given as N_1 X N_2 . The 2D-FFT not only improves the system level of the parallelism, but also reduces the demand for memory systems. The simulations were carried out on Modelsim 10.2 and the synthesis results on the Vertex-5 FPGA XC5VLX130T.

In the fourth chapter comparison analysis has been carried out between various digital modulation schemes in order to choose appropriate modulation scheme and the Bit Error rate was derived for different channels to choose the suitable one. This has been calculated theoretically and practically on Matlab software. And also the delay spread estimation was done i.e. how to estimate the delay in the presence of interference. The fifth chapter brings out the implementation of positioning the FFT window in the presence of interference. This has been implementing by three test cases as the receiver is ideal, Pedestrian or moving with some velocity in vehicle. And also the implementation of the same has been done for conventional OFDMA and FFT window positioning OFDMA in MATLAB in order to bring out the comparison between the BER VS Energy per bit.

7.1 SUMMARY OF RESULTS

The 2D-FFT algorithm was implemented i.e. based on the FFT-index the FFT size will be chosen and the time required to implement the 128-pt FFT ,512-pt FFT , 1024-pt FFT and 2048-pt FFT has been increased with the increase in the input FFT length in the software as well as hardware. A DDS-core was used to

generate a 50 MHz signal in which all the input points will be covered and based on the FFT index, FFT length was chosen and the 2D- FFT algorithm was applied. The 8-point FFT processor architecture consists of a single radix-2 butterfly (which is referred as the butterfly processing element), a dual-port FIFO RAM, a coefficient ROM, a controller and an address generation unit.

The FFT window positioning was done under three test cases i.e. when the delay is zero, delay=0.41 µs and delay = 2.51 µs. the same was simulated and synthesized on the software and the hardware as well. When the delay is zero, the time taken to calculate the 128-pt FFT was 7.37 µs for Modelsim software and 7.90 µs for vertex-5 FPGA hardware. Similarly for 512-pt FFT, 23.708 µs for software and 25.208 µs for the hardware, 1024-pt FFT is 51.257 µs and 53.857 µs, 2048-pt FFT remains to be 104.78 µs and 107.38 µs. The timing calculations were also derived for the delay 0.41 µs and 2.51 µs. when the delay was 0.41µs the, time taken for 512-pt FFT in Modelsim software was 23.710 µs and 25.212 µs for the Vertex-5 FPGA hardware. Similarly for 1024-pt FFT it was 51.253 µs and 53.890 µs for the software and hardware. For 2048-pt FFT the time taken to compute is 104.81 µs and 107.38 µs for software and hard ware. The time taken to calculate 128-pt FFT, 512-pt FFT, 1024-pt FFT and 2048-pt FFT was also calculated when the delay is 2.51 µs. the timings were almost same to the 1024-pt FFT. The results show that to process the FFT in the hardware it takes more time when compared to the simulation on the software and also the FFT calculation time for both hardware and software with all the delays is equal. The overall implementation of window positioned OFDMA was simulated and synthesized on FPGA hardware, which shows that the output signal is delayed by 1.6µs than the input signal ensuring that all the symbols have been received at the receiver.

The synthesis report which is generated contains all the information regarding the hardware device utilization and timing summary in terms of HDL synthesis like No of ROMs, Multipliers, Adders/ Subtractors, counters, registers etc. and Slice Logic Utilization like Number of Slice Registers and Number of Slice LUTs. IO

Utilization like Number of IOs, Number of BUFG/BUFGCTRLs and Number of DSP48Es. Timing summary was also generated and found to be Minimum period is 33.459ns, Maximum output required time after clock is 9.225ns and Maximum combinational path delay is 6.732ns.

Two cases were considered for the overall simulation of the OFDMA system i.e. one is conventional OFDMA and the FFT window positioned FFT. 3 GHz carrier was taken with the channel bandwidth of 20 MHz and sampling rate of 30.72 MHz. BER comparison was done various digital modulation schemes like 2-PSK, 64-PSK, 4-QAM and 64-QAM in which 64-PSK was found to have high BER with respect to Energy per bit i.e. 0.9485 at -5dB and 2-PSK has the lowest BER as 0.0204 at 10dB. For high data rate applications like DVB-H and DVB-T, 64-QAM has been chosen as the appropriate digital modulation scheme. Theoretical and practical BER was also calculated for QAM-64, and a maximum of 3% error was found between the both at10dB. Similarly comparison analysis was also done between the AWGN, Rayleigh and Rician fading channels in which a maximum BER was 0.45 at -5dB Eb/No for AWGN channel and 0.309 BER for Rayleigh fading channel at -5dB Eb/No and 0.004 at 15dB similarly 0.33 at -5dB and0.03 at 15dBfor Rician fading channel. And in the overall simulation of the window positioned FFT use of farrow filters has been done to introduce delay which gives the fractional delay. In the high data rate applications the BER must be as less as possible in order to reduce the signal interference. It is found that the BER for conventional OFDMA is 0.2 at 15dB SNR and 0.01 at 15dB SNR for window positioned FFT. Similarly BER of 0.007 for conventional OFDMA at 20dB and 0.0003 for window positioned FFT, with a significant improvement of 4.8%.

The FFT window positioning scheme of the Orthogonal Frequency Division Multiple Access was tested with all the possible delays and routes. The integration of delay introduction in the case of interference has given 100 % successful results of mitigation of the signal interference at the PHY layer of the OFDMA. The validation of the FFT window positioning was carried out in all

stages of the delay provided by the ITU. The research work of tracking loop enhancements for mitigating signal interference i.e. positioning of the FFT window in the presence of interference is a significant effort towards the mitigation of the signal interference and to have co-control over the FPGA chips.

7.2 FUTURE DIRECTIONS

The itemized several areas in this dissertation that can be extended for further research are as follows.

- One of the main draw backs of OFDM/OFDMA is Peak-to Average power ratio (PAPR) which causes the performance degradation. It is no doubt that there are many techniques introduced by many literatures using conventional OFDMA, FFT window positioned OFDMA will be a strong candidate as an alternative to reduce the PAPR. Some works on PAPR reduction are listed in [93], [94] and [95]. By using this method it will be more novelty because of variation in the implementation structure.

- Another future direction will be to use Super Imposed training Sequence of the pilot carriers instead of using cyclic prefix symbol during the transmission for the efficient channel estimation. Super imposed training will be done onto the carriers at the transmitter and this sequence is known to the receiver and hence there will be no use of cyclic prefix and the main advantage of such method is that bandwidth can be efficiently used. The disadvantage with such SIT based system is interference on the data subcarriers due to superimposed training sequence.

- The other direction might be the size of the digital modulation scheme, as the technology is increasing the same can be implemented for higher order scheme like 128-QAM, 256-QAM etc. and also for the other IEEE

standards and applications apart from OFDMA , the size of the FFT points can also be increased to 4096-pt FFT but when designing the hardware by using FPGA chip appropriate model should be selected as the designer's need to compete with synthesis tools availability, the number of operations performed and with the device utilization.